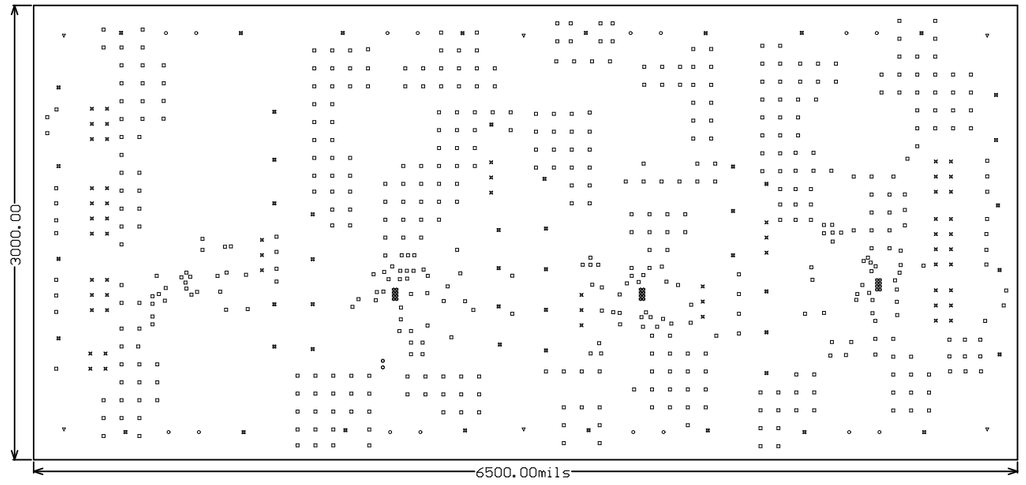
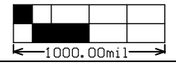
NOTE:
1. ALL VIAS ARE NON TENTED.
2. THIS IS NOT AN IMPEDANCE CONTROLLED BOARD.
3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED, PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING/COVERING" REQUIREMENTS.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1-Top Layer	Copper	2.80mil		
4	Dielectric 3	FR-4 HIGH TG	10.00mil	4.2	
5	L2-GND1	Copper	1.40mil		
6	Dielectric 2	FR-4 HIGH TG	35.00mil	4.2	
7	L3-PWR/SIG	Copper	1.40mil		
8	Dielectric1	FR-4 HIGH TG	10.00mil	4.2	
9	L4-Bottom Layer	Copper	2.80mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via/Pad
⌖	2	7.87mil (0.200mm)	PTH	L1-Top Layer - L4-Bottom Layer	Via
▽	6	125.98mil (3.200mm)	PTH	L1-Top Layer - L4-Bottom Layer	Pad
○	16	55.12mil (1.400mm)	PTH	L1-Top Layer - L4-Bottom Layer	Pad
✡	24	6.00mil (0.152mm)	PTH	L1-Top Layer - L4-Bottom Layer	Via
⊠	51	63.00mil (1.600mm)	PTH	L1-Top Layer - L4-Bottom Layer	Pad
⌑	59	40.00mil (1.016mm)	PTH	L1-Top Layer - L4-Bottom Layer	Pad
□	551	12.00mil (0.305mm)	PTH	L1-Top Layer - L4-Bottom Layer	Via
	709 Total				





DRILL TOLERANCE

FOR 6 MIL DRILL +0/- 6 MIL
FOR 7.87MIL DRILL +0/- 7.87 MIL
FOR 8MIL DRILL +0/- 8 MIL
FOR 12MIL DRILL +0/- 12 MIL
FOR PTH +/-3MILS

DESIGN INFORMATION

MIN. TRACK WIDTH: 9 MIL
MIN. CLEARANCE: 5.118 MIL
MIN. VIA PAD SIZE: 14 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] ALL 7.87 AND 12 MIL VIAS REQUIRE TENTING ON BOTH SIDES
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: TPS25947EVM
DESIGNED FOR: Public Release
FILE NAME: TPS25947EVM_PCB.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:TPS25947EVM	REV: E1	SVN REV: Not In VersionControl
LAYER NAME = [illegible]	TID #: N/A		
PLOT NAME =Fabrication Drawing	GENERATED : 23-08-2020 16:42:56		TEXAS INSTRUMENTS

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ENGINEER:	LAYOUT BY:
Praveen GD	TESSOLVE
SCALE: 1.00	ALTIUM DESIGNER VERSION: 18.1.9.240